TSMC-01-1693

April 16, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/785,524 02/24/04

Kuen-Chyr Lee et al.

A METHOD FOR IMPROVING THE ELECTRICAL CONTINUITY FOR A SILICON-GERMANIUM FILM ACROSS A SILICON/OXIDE/POLY-SILICON SURFACE USING A NOVEL TWO-TEMPERATURE PROCESS

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 26, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B. Ackerman 4/26/04

U.S. Patent 6,346,453 to Kovacic et al., "Method of Producing a Si-Ge Base Heterojunction Bipolar Device," describes a method for making an HBT using a sacrificial layer over a Si-Ge layer to protect an area for where an emitter is later formed.

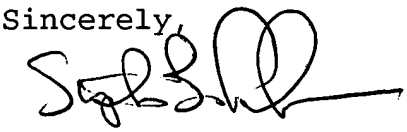
U.S. Patent 5,523,243 to Mohammad, "Method of Fabricating a Triple Heterojunction Bipolar Transistor," describes a method for making a triple HBT by forming a Si/Si-Ge superlattice for the base and a second superlattice for the emitter.

U.S. Patent 5,256,550 to Laderman et al., "Fabricating a Semiconductor Device with Strained Si1-x Gex Layer," describes a method for forming a strained SixGe1-x layer for the base of a bipolar transistor to improve the emitter injection efficiency.

U.S. Patent 6,251,738 to Huang, "Process for Forming a Silicon-Germanium Base of Heterojunction Bipolar Transistor," describes a method for making a Si-Ge base on a mesa and then removing the Si-Ge adjacent to the mesa.

U.S. Patent 5,951,757 to Dubbelday et al., "Method for Making Silicon Germanium Alloy and Electric Device Structures," describes a semiconductor structure which comprises at least one relaxed SiGe buffer formed on a silicon-on-insulator (SOI) substrate.

Sincerely,



Stephen B. Ackerman,
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Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
tsmc-01-1693	10/785,524
Applicant: Kuen-Chyr Lee et al.	
Filing Date: 02/24/04	Group Art Unit:

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6346453	2/12/02	Kovacic et al.	438	312	1/27/00
	5523243	6/4/96	Mohammad	437	31	6/8/94
	5256550	10/26/93	Laderman et al.	437	106	6/12/91
	6251738	6/26/01	Huang	438	312	1/10/00
	5951757	9/14/99	Dubbelday et al.	117	102	5/6/97

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.